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09/924,029	08/07/2001	Thane M. Larson	10012573-1	3018

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EXAMINER

ART UNIT PAPER NUMBER

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/924,029
Filing Date: August 07, 2001
Appellant(s): LARSON ET AL.

Thane M. Larson
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the remand issued from the Board on October 17, 2006 requiring a "Related proceedings appendix" section in the Examiner's answer and also requiring review of the 1449 submitted by Applicant on August 7, 2001. It is noted that another Examiner has been assigned to this application. This Examiner's answer is identical to the previous Examiner's Examiner answer mailed on February 15, 2006 except for the addition of a "Related proceedings appendix" section. Note an initialed and signed copy of the August 7, 2001 1449 is enclosed with the mailing of this Examiner's answer.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

NEW GROUND(S) OF REJECTION

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art and further in view of Verthein et al. US patent 6,678,284 and *Sides et al. US patent 6,363,449*.

Claims 8, 14, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art and further in view of Verthein et al. US patent 6,678,284, *Sides et al. US patent 6,363,449* and Liu US patent 6,185,110.

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The primary references and rejection rationale remain the same. *Sides* is now included in the rejection to support the Examiner's official notice that the intelligent platform management interface (IPMI) I²C bus was well known at the time of the invention. *Sides* was cited but not used in office action mailed 2/10/05.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Applicant Admitted Prior Art (Specification page 1)

6678284	Verthein et al.	1-2004
6363449	Sides et al.	3-2002
6185110	Liu	2-2201

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Applicant Admitted Prior Art and further in view of Verthein et al. US patent 6,678,284 and *Sides et al. US patent 6,363,449.*

As per claim 1, a server system with plurality of host processing cards and manual assignment of IP addresses to the host processing cards are admitted prior art (Applicant's specification page 1). The admitted prior art does not have an integrated management card with user interface for manual assignment of the IP addresses. The admitted prior art uses a separate

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terminal connected via RS-232 interface for setting up the IP address information. In similar field of invention, Verthein teaches providing a general purpose computing card in a server chassis coupled to plurality of network service cards via an internal chassis bus (col. 2 lines 55-62). The general purpose computing card is installed with management software (col.3 line 1) such that a user can directly interact with it (col.4 line 31-35). This provides for improve network management and reduces access and processing time. (See Verthein col.2 line 68 to col.3 line 8). Hence, given the teaching of Verthein, one of ordinary skill in the art would have been motivated at the time of the invention to have a management card in the chassis of the Admitted Prior Art server system for managing the host processor cards in the chassis because it would have eliminated the need for connecting an external terminal to the chassis and improved management and reduced access time to the host processing cards in the chassis (Verthein col.3 lines 1-8).

As per claims 2-3, the references are silent on the use of IPMI I2C bus. However, IPMI I2C bus is well known in the art (see Sides col.2 line 59 to col.3 line 59). IPMI is designed specifically for management of hardware (Sides col.3 lines 5-15). I2C bus is efficient because it requires only two signal lines. Hence, it would have been obvious for one of ordinary skill in the art to have used IPMI I2C bus for managing the cards in the Admitted Prior Art system as modified because it would have used minimal number of signal lines in the chassis.

As per claim 4, since Admitted Prior Art as modified has the processing card for assigning IP addresses to the host processing cards in the chassis via IPMI I2C bus. IPMI is specifically designed for managing hardware (Side col.3 lines 5-15). Hence, it would have been obvious for one of ordinary skill in the art to use the card to send other configuration data or commands via the IPMI

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I2C bus as required so as enabling a user to effectively manage the host processing cards in the chassis.

As per claim 5, manual assignment of IP address to the host processing card is in the admitted prior (see Applicant's specification page 1).

As per claim 6, it is well known in the art that configuration of IP address include providing address of any gateway, subnet masks, host name, etc. to the device. Hence, providing these information during configuration of the host processing cards would have been obvious to one of ordinary skill in the art.

As per claim 7, Verthein teaches providing the card with LAN interface (fig.2 #42), and serial interface (fig.2 #36, 34).

As per claims 9-13, they are rejected under similar rationale as for claims 1-6 above. The usage of I2C bus would have been obvious to one of ordinary skill in the art as stated in the rejection of claims 2-3 above.

As per claim 15-19, they are method corresponding the system claims 1-6. Hence, they are rejected under similar rationale as claims 1-6 above.

Claims 8, 14, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art and further in view of Verthein et al. US patent 6,678,284, Sides et al. US patent 6,363,449 and Liu US patent 6,185,110.

As per claim 8, Verthein does not teach providing LCD panel mounted on the server chassis. Verthein provides an interface to an external display (fig.2 #32). However, in similar field of invention, Liu teaches an improved chassis system by providing mounting of LCD panel on the

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server chassis (see abstract, fig. 1, col. 1 lines 29-40). Hence, it would have been obvious for one of ordinary skill in the art to use the LCD of Liu with the Admitted Prior Art system as modified because it would have enabled the display to be integrated on the server chassis and eliminating the problem of connecting external devices to the server system (Liu col. 2 lines 1-5).

As per claims 14 and 20, they are rejected under similar rationale as for claim 8 above. Verthien teaches providing the card with LAN interface (fig. 2 #42), and serial interface (fig. 2 #36, 34).

(10) Response to Argument

Applicant argued that Verthein does not teach and Applicant did not admit as prior art the limitation “the management card including at least one user interface for receiving network address from a user.” and transmission of the assigned IP address to the host processing cards via the chassis bus. The argument is not persuasive.

As admitted by applicant in the background disclosure, it is known in the art to manually assign IP to host processing cards. This is a conventional configuration procedure. The admitted prior art system uses a terminal connected via a RS-323 interface to configure the host processing cards in the chassis. The prior art system inherently has a user interface for a user to enter the IP address for transmission to the host processing cards in the chassis.

Verthein teaches an improved method for management of a chassis by providing a general computing card connected to the internal chassis bus for carrying out management function of the cards in the chassis [see col. 2 lines 55-60]. It is clear from Verthein teaching that configuration information is transmitted from the general computing card to processing cards in

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the chassis via the internal chassis bus (see col.3 lines 1-7 and 9-14). Verthein discloses that his invention provides reduce access time to the chassis (col.3 lines 5-8). Hence, given the teaching of Verthein, it would have been obvious for one of ordinary skill in the art at the time of the invention to use Verthein general computing card to manage a cards in a chassis such as that of the Admitted Prior Art system because it would have provided management function within the chassis and reduces access time to the chassis (Verthein col.3 lines 5-8).

It is not clear from the claim language whether “user inferface” means the input hardware (i.e. keyboard, mouse) or the software display that permit a user to enter information. However, both interpretations read on the prior art applied. Verthein discloses providing user interface ports for connection of keyboard, mouse and a display so that a user can directly access and input data to the general computing card (col.4 lines 31-36). Since Admitted Prior Art system is now modified to have a general computing card of Verthein in the chassis for management of the host processing cards instead of using an external RS232 terminal, it is obvious that the ‘user interface’ (e.g. the program to permit a user to manually enter IP address and manage the host processing cards of the Admitted Prior Art) would be installed or rewritten to run in the general processing card. Therefore, the system as modified in the rejection would have had a user interface (input hardware and software) for receiving IP address from the user as claimed.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner’s answer.

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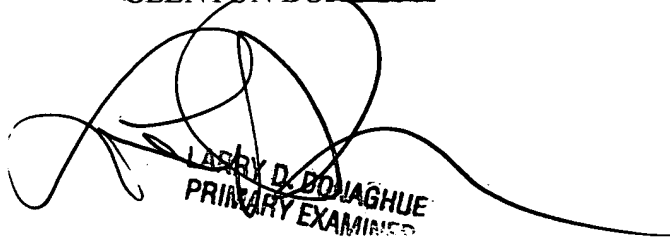
Respectfully submitted,



Sean Reilly

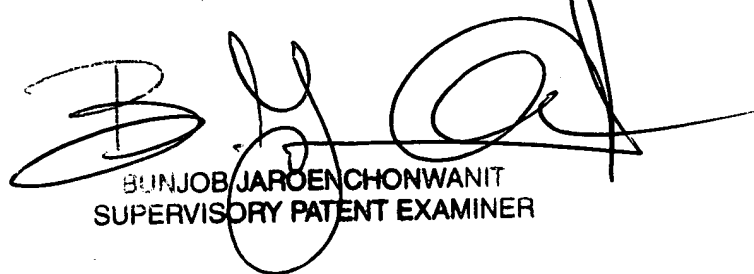
Conferees:

~~GREEN FOR DISMISS~~



LARRY D. DONAGHUE
PRIMARY EXAMINER

JAROENCHONWANIT BUNJOB



BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER

Approved.



PAUL SEWELL
ACTING DIRECTOR